AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A system for synchronous sampling of analog signal inputs, using an externally generated encoded time signal, comprising:

an input for receiving said externally generated encoded time signal ~~input~~ suitable for ensuring accurate time-of-day clock synchronization, wherein the time signal covers a predetermined time period;

an edge detector responsive to the encoded time signal to produce a series of pulses based on the edges of the encoded time signal; and

a phase-locked loop assembly producing an output sampling synchronization signal which is phased-locked to said pulses at the output of the edge detector, such that the output sampling synchronization signal occurs at the beginning of each predetermined time period with successive synchronization signals being evenly spaced in the interval between the beginning of each successive predetermined time.

2. (Original) The system of claim 1, wherein the time signal is an IRIG-B time signal.

3. (Original) The system of claim 1, wherein the phase-locked-loop is locked at 1 kHz and the output sampling synchronization signal is an integral multiple of 1 kHz.

4. (Original) The system of claim 1, wherein the predetermined time period is one second.

5. (Original) The system of claim 1, wherein the edge detector detects only rising edges of the encoded time signal and produces an output based thereon.

6. (Original) The system of claim 1, wherein the edge detector detects both rising and falling edges of the encoded time signal and produces an output based thereon.

7. (Currently Amended) The system of claim 1, wherein the encoded time signal includes a bit which identifies the beginning of each frame of the encoded time signal.

8. (Original) The system of claim 1, wherein the phase-locked-loop assembly includes a phase detector, a filter responsive to the output of the phase detector and a counter responsive to the output of the filter for producing the output sampling synchronization pulses, and wherein the phase-locked-loop assembly further includes a feedback circuit responsive to the output signal of the counter for feeding back the output signal to the phase detector, which produces an output signal by which the counter is adjusted to lock the sampling synchronization signal to the encoded time signal.

9. (Currently Amended) A system for synchronous control of a selected operation, using an externally generated encoded time signal, comprising:

an input for receiving the externally generated encoded time signal, suitable for ensuring ~~insuring~~ accurate time-of-day clock synchronization, wherein the time signal covers a predetermined time period;

an edge detector responsive to the encoded time signal to produce a series of pulses based on the edges of the encoded time signal; and

an assembly which produces an output synchronization signal for [[a]] the selected operation, locked to the output of the edge detector, such that the output sampling synchronization signal occurs at the beginning of each predetermined time period with successive synchronization signals being evenly spaced in the interval between the beginning of each successive predetermined time.

10. (Original) The system of claim 9, wherein the time signal is an IRIG-B time signal.

11. (Original) The system of claim 9, wherein the assembly is a phase-locked loop.

12. (Currently Amended) A system for sampling analog signal inputs, using an externally generated encoded time signal, comprising:

an input for receiving the externally generated encoded time signal, suitable for ensuring

accurate time-of-day clock information, wherein the time signal covers a predetermined time period;

an edge detector responsive to the encoded time signal to produce a series of pulses based on the edges of the encoded time signal; and

a phase-locked loop assembly which produces an output sampling signal which is phase-locked to the output-of the edge detector, such that the output sampling synchronization signal occurs at the beginning of each predetermined time period with successive sampling signals being evenly spaced in the interval between the beginning of each successive predetermined time.

13. (Original) The system of claim 12, wherein the time signal is an IRIG-B time signal.